**Analog Integrated Circuit Lab Manual**

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| **S.No** | **List Of Experiments** | **Page No** |
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| 4. | Demonstrate the working of transistorized Multi-vibrator.  (Astable/ Mono/Bistable) |  |
| 5. | Demonstrate the working of Class C tuned amplifier. |  |
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**DESIGN AND ANALYSIS OF VOLTAGE DIVIDER BIAS**

Experiment No: …………….

Date: ……. /……. /……………

**Aim**: To design and analyze the voltage divider bias.

***Equipment and Components Required***:

Dual Power supply (0-30V), Oscilloscope (0-30MHz), Transistor BC107 , Function Generator (0-3MHz),Resistor -- kΩ, ----- kΩ, ---kΩ, ---- kΩ, ---kΩ,, Capacitor --μF, ----μF,5 ---µf, Breadboard, Connecting wires

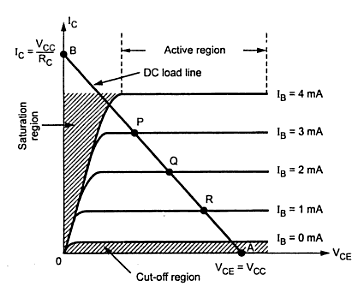
***Theory:***

Biasing is to fix the Q – point in the middle of the active region we go for Biasing. The proper flow of zero signal collector current and the maintenance of proper collector emitter voltage during the passage of signal is known as transistor biasing.

When a transistor is biased properly, it works efficiently and produces no distortion in the output signal and thus operating point can be maintained stable. The following are the factors that affect the stability of the operating point,

a. Transistor current gain factor - Change of hfe/β due to replacement of transistors.

b. Thermal variations - ICO, VBE, βdc



***In the circuit diagram***

1. R1 , R2 – Potential divider

2. If Ic increases , IE also increases it reduces the voltage drop across base and emitter (VBE)

3. Due to reduction in VBE  , base current and collector current get reduced.

4. Negative feedback exists in the emitter bias circuit.

**DESIGN:**

Given specifications:

VCC= --- V, IC= ---- mA, AV= ----, fI = --- kHz, S= -- , hFE= ---, β=----

The feedback factor, β= - 1/RF= +1/0.4=2.5KΏ

**(i) To calculate RC:**

The voltage gain is given by,

AV= -hfe (RC|| RF) / hie

re = 26mV / IE

h ie = β re = -----

Apply KVL to output loop,

VCC= IC RC + VCE+ IE RE ----- (1)

Where VE = IE RE (IC= IE)

VE= VCC / 10= 1V

Therefore RE= -----

VCE= VCC/2= 5V

From equation (1), RC= -----KΏ

**(ii) To calculate R1&R2:**

S=1+ (RB/RE)

RB= (S-1) RE= R1 || R2 = ----KΏ

RB= R 1R2 / R1+ R2------- (2)

VB= VBE + VE = 0.7+ 1= 1.7V

VB= VCC R2 / R1+ R2 ------- (3)

Solving equation (2) & (3),

R1= -----KΏ & R2= ------KΏ

**(iii) To calculate Resistance:**

Output resistance is given by,

RO= RC || RF

RO= -----KΏ

input impedance is given by,

Ri = (RB|| RF) || hie = ------KΏ

Trans-resistance is given by,

Rm= -hfe (RB|| RF)( RC || RF) / (RB|| RF)+ hie

Rm= ------KΏ

**AC parameter with feedback network:**

**(i) Input Impedance**:

Rif = Ri /D (where D= 1+β Rm)

Therefore D = ------

Rif= ====

Input coupling capacitor is given by,

Xci= R­if / 10= 2.4 (since XCi << Rif)

Ci = 1/ 2пfXCi = -------µf

**(ii) Output impedance:**

ROf= RO/ D = ------

Output coupling capacitor:

XCO= Rof /10= 5.2

CO = 1/ 2пfXCO= 30µf

**(iii) Emitter capacitor:**

XCE << R’E = R’/10

R’E= RE|| {( hie +RB) / (1+hfe)}

XCE= ------

Therefore CE= -------µf

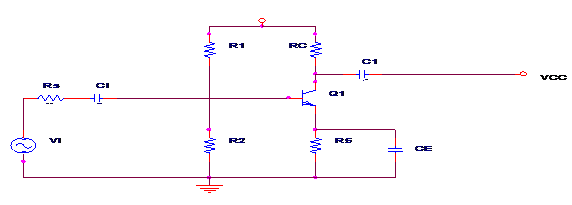
***Experiment Procedure:***

* **Connections are made as per circuit diagram.**
* **Keep the input voltage constant at 20mV peak-peak and 1 kHz frequency. For different values of load resistance, note down the output voltage and calculate the gain by using the expression**
  + **Av= 20log(V0/ Vi) dB**
* **Add the emitter bypass capacitor and repeat STEP 2.And observe the effect of Feedback on the gain of the amplifier**
* **For plotting the frequency the input voltage is kept constant at 20mV peak-peak and the frequency is varied from 100Hz to 1MHz.**
* **5.**    **Note down the value of output voltage for each frequency. All the readings are tabulated and the voltage gain in dB is calculated by using expression**

**Av= 20 log(V0/ Vi) dB**

* **A graph is drawn by taking frequency on X-axis and gain on Y-axis on semi log graph sheet**
* **The Bandwidth of the amplifier is calculated from the graph using the expression Bandwidth B.W = f2 – f1.**
* **Where f1 is lower cut off frequency of CE amplifier**
  + **f 2is upper cut off frequency of CE  amplifier**
* **The gain-bandwidth product of the amplifier is calculated by using the expression**
  + **Gain-Bandwidth Product = 3-dB mid band gain X Bandwidth.**

***Circuit diagram:***

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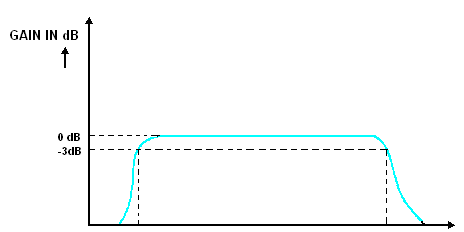
***WORKSHEET***

**Frquency Response:   Vi = ------mV**

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| --- | --- | --- | --- | --- |
| **S.NO** | **Frequency (Hz)** | **Output Voltage (Vo­)** | **Gain A = Vo­/Vi** | **Gain in dB**  **20log(Vo­/Vi)** |
|  |  |  |  |  |

**MODEL WAVEFORMS:**

**MODEL GRAPH:**



**f 1 f2 f (Hz)**

***V-I characteristics of Voltage divider bias:***

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***Conclusion:***

**The voltage gain and frequency response of the amplifier are obtained. Also gain-bandwidth product of the amplifier is calculated.**

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**DESIGN AND ANALYSIS OF RC PHASE SHIFT OSCILLATOR**

**Aim**: To design and analyze the RC Phase Shift Oscillator.

***Equipment and Components Required***:

Dual Power supply (0-30V), Oscilloscope (0-30MHz), Transistor BC107 , Resistor ------KΩ, ----Ω, -----KΩ, ------KΩ , Capacitor ------µF , -----µF , Breadboard, Connecting wires

***Theory:***

The RC phase shift oscillators basically consist of an amplifier and feedback network. The feedback network consists of resistors and capacitors arranged in cascade to produce oscillations. For a circuit to act as an oscillator certain criteria's need to be satisfied. This criterion is called Barkhausen Criteria. According to this criteria an amplifier stage will act as an oscillator.    
  
1) The signal feedback from the output to the input is in same phase with the actual input.  
  
2) The factor Aβ =1, where A is the amplifier gain and β is the feedback factor   
  
  
The resistors R1 and R2 form the voltage divider network. Rc is used for providing collector bias and it act as the load the Re resistor provide thermal stabilization. The capacitor Ce is called the bypass capacitor as it is used to bypass frequency components produced at the emitter terminal to the ground. This capacitor have a great role in gain stability because if frequency components were allowed to pass through Re resistor then the drop in Re increases and this could result in negative feed backing and can reduce the gain of the amplifier.

When the Vcc is provided any circuit imbalance could produce small base current and this will be amplified at the collector terminal with 180­0 phase shift. The collector terminal is connected with 3 phase shift networks (RC) which produce approximately 600 phase shift each and to their combined effect produces another 180 degree phase shift. The last resistor R is connected to the base of the amplifier. This act as the feedback path so the signal feedback from the phase shift stage is now (3600 phase different or) in phase with the input hence the Barkhausen Criterion 1 is satisfied. The phase feedback network is designed to make the product Aβ=1 and hence both the criteria's were satisfied and the circuit act as an oscillator.  
From the derivations the frequency of an RC oscillator can be obtained as f =1/(2∏RC√ (6+4Rc/R)) and the hFE of the transistor required is given by hFE >= 23+29(Rc/R)+4(R/Rc) from this equation the minimum hFE required is 29.

**Design of a practical RC phase shift oscillator**

**Output requirement:**

 Sine wave with 10Vpp and frequency 500Hz

**Selection of BJT :** Select transistor BC 107 as its minimum hfe is 100

**Design of Rc and Re :** Let the Vcc is chosen to be 20% more than the required output swing therefore Vcc= -----v . Let this voltage be divided as follows 40% across Rc, 50% across BJT and 10% across Re therefore VRc= ----V ,VRe= ----V, VCE= ---V , Ic = ----(collector current from datasheet)

Rc=V~~Rc~~/Ic=----KΩ  
Re=VRe/Ie=VRe/Ic=---Ω,

**Design of R1 and R2:** Let the current through R1 be 10 Ib and current through R2 be 9 Ib this assumption is made in order to prevent loading of the voltage divider by the base current  
Ib=Ic/hfe=------   
VR2=VBE+VRe=.-------

VR1=Vcc-VR2=----------  
R1=VR1/10Ib=--------   
R2=VR2/9Ib=---------  
  
**Design of Ce:** Ce is the bypass capacitor let the lowest frequency that it bypass should be 100Hz   
The impedance of the capacitor XCe<=Re/10 (standard rule) The resonant frequency of any RC network is given by

f=1/(2πRC)   
Here R=Re/10= ----- ,F= ----Hz so from this C=Ce>=1/(2πfRe) = -----µF ,   
  
**Design of Phase shift network:**

Since our required frequency of oscillation is 500Hz the phase shift network should provide 180 degree phase shift to this frequency.

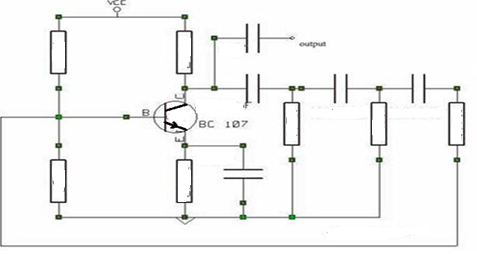
From the frequency equation of the phase shift network f=1/(2∏RC√ (6+4Rc/R)) where F=500Hz , Take R =4.7K to limit collector current from this equation C can be found out

C=1/(2πRf√(6+4Rc/R))=-------µF

***Experiment Procedure:***

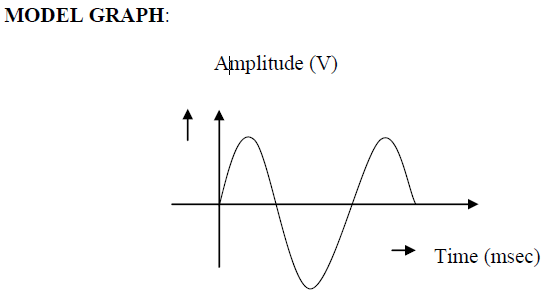
* Connect the circuit as per the circuit diagram.
* Measure the frequency of oscillation (fo) and the amplitude of the output voltage.
* Measure and draw the waveforms
* Observe the effect of variation of the potentiometer on the frequency of oscillation.
* Observe the effect of the variation of RE and RB on fo.

***Circuit diagram :***

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| **Amplitude in Volt** | **Time in msec** |
|  |  |



***V-I characteristics of RC phase shift oscillator:***

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***Conclusion:***

RC phase shift oscillator designed and output waveform is plotted.

***Frequency of oscillation: -------***

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**DESIGN AND ANALYSIS OF HARTLEY OSCILLATOR**

Experiment No: …………….

Date: ……. /……. /……………

**Aim**: To construct Hartley oscillator using a transistor, to find out the frequency of

oscillation and comparing it to that of theoretical frequency..

***Equipment and Components Required***:

Dual Power supply (0-30V), Oscilloscope (0-30MHz), Transistor BC107, Resistor 2k Ω,

1K Ω,100 k Ω,22kΩ , Capacitor 3.2nf ,0.1μF,0.01μF , Breadboard, Connecting wires

***Theory:***

The Hartley oscillator is an [electronic oscillator](https://en.wikipedia.org/wiki/Electronic_oscillator) [circuit](https://en.wikipedia.org/wiki/Electronic_circuit) in which the oscillation frequency is determined by a [tuned circuit](https://en.wikipedia.org/wiki/Tuned_circuit) consisting of [capacitors](https://en.wikipedia.org/wiki/Capacitor) and [inductors](https://en.wikipedia.org/wiki/Inductor), that is, an LC oscillator. Hartley oscillator is a one type of sine wave generator. Hartley Oscillator have two major parts namely – amplifier part and feedback part. The amplifier part has a typically CE amplifier with voltage divider bias. In the feedback path, there is a LCL network. The feedback network generally provides a fraction of output as feedback. It is a high frequency generator.

When the collector supply voltage Vcc is switched on, collector current starts rising and charges the capacitor C. When this capacitor is fully charged, it discharges through coils L1 and L2, setting up damped harmonic oscillations in the tank circuit. The oscillatory current in the tank circuit produces an a.c. voltage across L1 which *is* applied to the base emitter junction of the transistor and appears in the amplified form in the collector circuit. Feedback of energy from output (collector emitter circuit) to input (base-emitter circuit is) accomplished through auto transformer action. The output of the

amplifier is applied across the inductor L1, and the voltage across L2 forms the feedback voltage. The coil L1, is inductively coupled to coil L2, and the combination acts as an auto-transformer. This energy supplied to the tank circuit overcomes the losses occurring in it. Consequently the oscillations are sustained in the circuit. The energy supplied to the tank circuit is in phase with the generated oscillations. The phase difference between the voltages across L1 and that across L2 is always 180°

because the centre of the two is grounded. A further phase of 180° is introduced between the input and output voltages by the transistor itself. Thus the total phase shift becomes 3600 (or zero), thereby making the feedback positive or regenerative which is essential for oscillations.

**Design of a practical RC phase shift oscillator**

**Output requirement:**

 Sine wave with 10Vpp and frequency 500Hz

**Selection of BJT :** Select transistor BC 107 as its minimum hfe is 100

**Design of feed back Network:**

Given L1= L2=10mH, f=20 KHz, VCC=12V, IC=3mA, S=12

f = 1/2∏

C= 3.2nf

**Amplifier design:**

**(i)** **Selection of RC:**

Gain formula is,

AV= - hfe RLeff / hie

Assume VCE=VCC/2 (Transistor active)

VCE= 12/2= 6V

VE=IERE= VCC/10=1.2V

VCC=ICRC + VCE + IERE

RC= (VCC- VCE -IERE) / IC

Therefore RC = 1.6KΩ=2 KΩ

**(ii)** **Selection of RE:**

IC= IE=3mA

RE= VE/IE

RE= 1.2 / 3x10-3=400 Ω=1KΩ

**(iii)** **Selection of R1 & R2:**

Stability factor S=12

S=1+ (RB/ RE)

12=1+ (RB/1x103)

RB=11K

Using potential divider rule,

RB=R1R2 / R1+R2 & VB= (R2/ R1+R2) VCC

RB /R1= R2/ R1+R2

Therefore RB/R1= VB/VCC

VB=VBE+ VE= 0.7+1.2=1.9V=2V

R1= (VCC/ VB )RB

R1= (12/2)x 11x103=66KΩ=100KΩ

VB/VCC =R2 / R1+R2

2/ 12=R2 / 100x103+R2

(100x103)+R2=R2/0.16=19KΩ

R2=19KΩ=22 KΩ

**(iv)Output capacitance (CO):**

XCO=RC/10=2x103/10=200

1/2∏fCO=200

CO=1/2x3.14x20x103x200

CO=0.039=0.01µf

**(v)** **Input capacitance (Ci):**

XCin= RB/10=11x103/10=1.1x103

1/2∏fCin=1.1x103

Cin=1/2x3.14x20x103x1.1x103

Cin= 0.007=0.01µf

**(vi) By pass Capacitance (CE):**

XCE=RE/10=1x103/10=100

1/2∏fCE=100

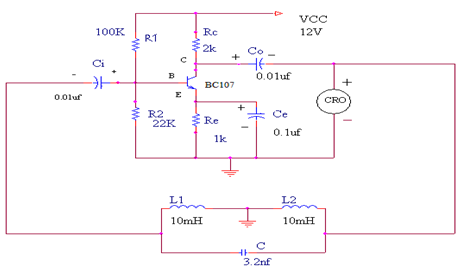
CE= 1/2x3.14x20x103x100

CE = 0.079µf = 0.1µf

***Experiment Procedure:***

* Connect the circuit as per the circuit diagram.
* Set VCC = 12V.
* For the given supply the amplitude and time period is measured from CRO.
* Frequency of oscillation is calculated by the formula f=1/T
* Verify it with theoretical frequency, f= 1/2∏ () Amplitude Vs time graph is drawn.

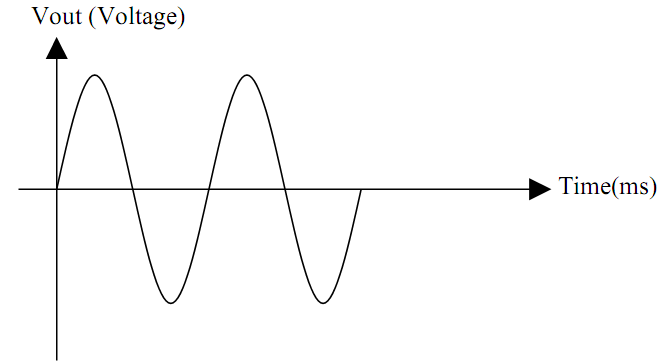
***Circuit diagram :***

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***WORKSHEET***

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| **Amplitude (V)** | **Time(μs)** | **Frequency (Hz)** |
|  |  |  |

**MODEL GRAPH:**

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***V-I characteristics of RC phase shift oscillator:***

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***Conclusion:***

Thus the Hartley oscillator is designed and constructed for the  given frequency.

                      Theoretical frequency:

                      Practical frequency **:**

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